

UB-SUFFIX SERIES CMOS GATES

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices
- · Formerly Listed without UB Suffix

LOGIC DIAGRAMS MC14011UB MC14002UB MC14001UB Quad 2-Input NOR Gate Quad 2-Input NAND Gate Dual 4-Input NOR Gate 12. 13 13 MC14025UB MC14023UB MC14012UB Triple 3-Input NOR Gate Triple 3-Input NAND Gate Dual 4-Input NAND Gate 12. 12 13 -VDD = Pin 14 VSS = Pin 7 for All Devices

MC14001UB

Quad 2-Input NOR Gate

MC14002UB

Dual 4-Input NOR Gate

MC14011UB

Quad 2-Input NAND Gate

MC14012UB

Dual 4-Input NAND Gate

MC14023UB

Triple 3-Input NAND Gate

MC14025UB

Triple 3-Input NOR Gate

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

UB-SERIES GATES

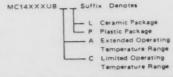




CERAMIC PACKAGE

P SUFFIX CASE 646

ORDERING INFORMATION



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either Vss or Vppl

CMOS UB-SERIES GA-

MAXIMUM RATINGS (Voltages

Rating

DC Supply Voltage

Input Voltage, All Inputs

DC Current Drain per Pin

Operating Temperature Range

Storage Temperature Range

ELECTRICAL CHARACTER

Characteristic

.0.

Output Voltage

Vin . VDD or 0

Vin = 0 ot VDD

Input Voltage# (VO = 4.5 Vdc)

(VO = 9.0 Vdc) (VO = 13.5 Vdc)

(Vo = 0.5 Vdc)

(VO = 1.0 Vdc) (VO = 1.5 Vdc)

Output Drive Current (AL Dev

(VOH = 2.5 Vdc)

(VOH 4.6 Vdc)

(VOH = 9.5 Vdc) (VOH = 13.5 Vdc)

(VOL = 0.4 Vdc) (VOL = 0.5 Vdc)

(VOL = 1.5 Vdc)

(VOH = 25 Vdc) (VOH = 46 Vdc)

(VOH = 9.5 Vdc) (VOH = 13.5 Vdc)

(VOL = 0.4 Vdc) (VOL = 0.5 Vdc)

(VOL = 1.5 Vdc)

Input Current (AL Device

Input Current ICL/CP De

Input Capacitance (V in = 0)

Quiescent Current (AL C

(Per Package)

Quiescent Current ICL/

Total Supply Current* (Dynamic plus Quit Per Gate, CL = 50

*Tlow = -55°C for A Thigh = + 125°C for

#Noise immunity spe Noise immunity spe Noise Mergin for bo 0.5 Vdc min @ 1.0 Vdc min @ 1.0 Vdc min @



QUAD 2-INPUT "NAND" GATE

The MC14011B and MC14011UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14011B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14011B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4011B and CD4011UB

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	05 to +18	Vdc
Input Voltage, All Inputs	Vin	-05 to VDD -05	Vdc
DC Current Drain per Pin	1	10	mAdd
Operating Temperature Range AL Device	TA	-55 to +125 -40 to +85	оС
Storage Temperature Range	Tstq	-65 to +150	oC

See the MC14001B data sheet for complete characteristics of the B-Series device.

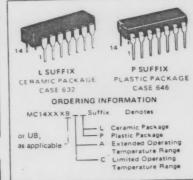
See the MC14001UB data sheet for complete characteristics for the UB device.

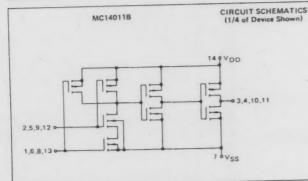
MC14011B MC14011UB

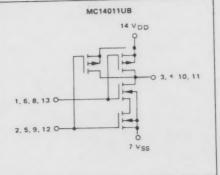
CMOS SSI

LOW POWER COMPLEMENTARY MOSI

QUAD 2-INPUT "NAND" GATE







This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that nor mall precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be field to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTO

DUAL 4-IN

The MC14012B and MC14 channel enhancement mode (Complementary MOS). T dissipation and/or high nois

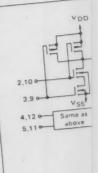
- Quiescent Current = 0.5
- Noise Immunity = 45%
- Supply Voltage Range
- All Outputs Buffered (
- Capable of Driving Tw Schottky TTL Load of ature Range. (MC1401
- Double Diode Protect
- · Pin-for-Pin Replacem

MAXIMUM RATINGS (Voltage

DC Supply Voltage
Input Voltage All Inputs
DC Current Drain per Pin
Operating Temperature Range

Storage Temperature Range

See the MC14001E B-Series device. See the MC14001L UB device.



This device contains on to high static voltages mal precautions by taking maximum rated voltain



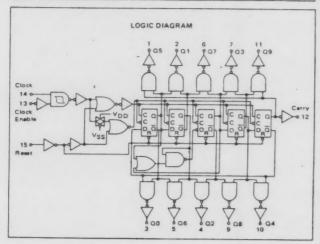
DECADE COUNTER/DIVIDER

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positivegoing edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
 Carry Out Output for Cascading
- 12 MHz (typical) Operation @ VDD = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
 Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B

MAXIMUM RATINGS (Voltages reference

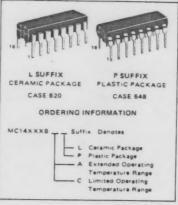
Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0 5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0 5 to VDD + 05	Vdc
DC Current Drain per Pin	1	' 10	mAdo
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	Tstg	-65 to +150	°C



MC14017B

CMOS MSI

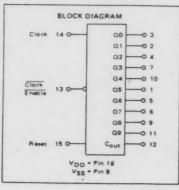
(LOW POWER COMPLEMENTARY MOS) DECADE COUNTER/DIVIDER



FUNCTIONAL TRUTH TABLE

CLOCK	CLOCK	RESET	DECODE OUTPUT = n
0	X	0	n
×	1	0	n
×	×	1	00
5	0	0	n+1
~	×	0	n
×	5	0	n
1	~	0	n+1

X = Don't Care If n <5 Carry = "1", Otherwise = "0"



MC14017B

ELECTRICAL CHARACTERIS

Characteristic	
Output vortage	"0" Leve
Vin VDD or 0	
	"1" Lev
Vin 0 or VDD	
Input Voltage#	"0" L
(Va = 4.5 or 0.5 Vdc)	
(Vo = 9.0 or 1.0 Vdc)	
(Vo = 13.5 or 1.5 Vdc)	
(VO = 0.5 or 4.5 Vdc)	
(Vo = 1.0 or 9.0 Vdc)	
(VO = 1.5 or 13.5 Vdc	1
Output Drive Current (AL	Device
(VOH = 2.5 Vdc)	Source
(Vau = 4.6 Vdc)	
(VOU = 9.5 Vdc)	
(VOH = 13.5 Vdc)	
(VOL = 0.4 Vdc)	Sink
1 (Va) = 0.5 Vdc)	
(VOI = 1.5 Vdc)	
Output Drive Current (CL	/CP Dev
(VOH = 2.5 Vdc)	Source
(VOH = 4.6 Vdc)	
(VOH = 9.5 Vdc)	
(VOH = 13.5 Vdc)	
(Vol = 0.4 Vdc)	Sink
(Va) = 0.5 Vdc)	
(VOI = 1.5 AOC)	
Input Current (AL Device	:e)
Input Current (CL/CP D	evice)

(Vin = 0)
Quiescent Current (AL Device) (Per Package)

input Capacitance

Quiescent Current ICL/CP Device (Per Package)

Total Supply Current "1 (Dynamic plus Quiescent, Per Package) (CL = 50 pF on all outputs,

buffers switching!

*Tlow = -55°C for AL Device
Thigh = +125°C for AL Dev
=Noise immunity specified fa Noise Margin for both "1" a

tTo calculate total supply cu IT(CL) = IT(50 pF) + where: IT is in µA (per par **The formulas given are for

the inc voltage advised to avo than i



MC140

Oout

MOTOROLA

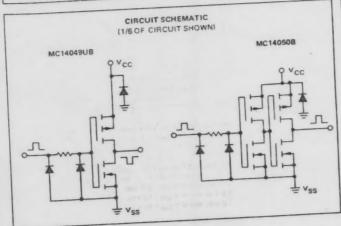
HEX BUFFERS

The MC14049UB hex inverter/buffer and MC14050B noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, VCC. The input-signal high level (VIH) can exceed the VCC supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (VCC = 5.0 V, VOL ≤ 0.4 V, IOL ≥ 3.2 mA). Note that pin 16 is not connected internally on these devices; consequently connections to this terminal will not affect circuit operation.

- High Source and Sink Currents
- · High-to-Low Level Converter
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Meets JEDEC UB Specifications—MC14049UB Meets JEDEC B Specification—MC14050B

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8)

MAXIMUM RATINGS (Voltages to	Symbol	Value	Unit
Rating	-	-0.5 to +18	Vdc
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	10	mAdo
DC Current Drain per Input Pin		45	mAdd
DC Current Drain per Output Pin	1	-55 to +125	, C
Consating Temperature Range AL Device	TA	-40 to +85	
CL/CP Device	Tstg	-65 to +150	, c
Storage Temperature Range	31.9		



MC14049UB MC14050B

CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

HEX BUFFERS

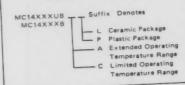
Inverting - MC14049UB Noninverting - MC14050B



L SUFFIX CERAMIC PACKAGE CASE 620

PSUFFIX PLASTIC PACKAGE CASE 648

ORDERING INFORMATION



LOGIC DIAGRAMS

MC14049UB	MC14050B
3-0-2	3-2
54	5 — 4
7-0-6	7 — 6
9-0-10	910
11-0-12	11 — 12
14-0-15	14 — 15
NC = Pin 13, 16	NC = Pin 13, 16
VSS = Pin 8 VCC = Pin 1	VSS = Pin 8 VCC = Pin 1
-	



MC14075B

M

TRIPLE 3-INPUT "OR" GATE

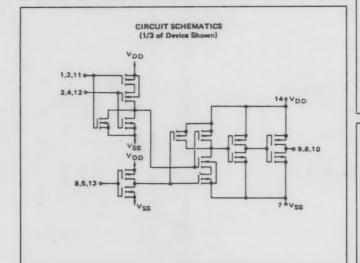
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD40758

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD .	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to VDD +0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	Tstg	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.



CMOS SSI

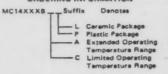
(LOW-POWER COMPLEMENTARY MOSI

TRIPLE 3-INPUT "OR" GATE

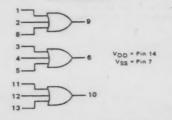


L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX PLASTIC PACKAGE CASE 646

ORDERING INFORMATION



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < (Vin or Vout) < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either Vss or Vpp).

The MC140 operating synches able inputs in bus organize outputs to be are inhibited fundisturbed. A

- four flip-flops inputs.

 Three-State
- Fully Indes
 Two Modes
 Asynchrone
- For Bus Bu
- Quiescent (
- Supply Vol
- Capable of Schottky 7 ature Rang

MAXIMUM RATIN

DC Supply Voltage Input Voltage, All Inp DC Current Drain per Operating Temperatur

Storage Temperature

When either output impedance state; how X = Don't Care.



MC14082B

DUAL 4-INPUT "AND" GATE

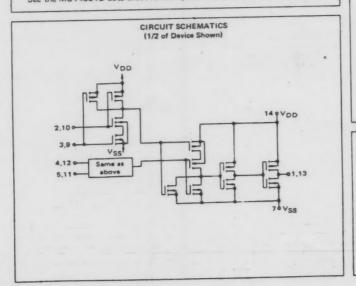
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of Vpp typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD40828

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to VDD -0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range AL Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.



CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "AND" GATE



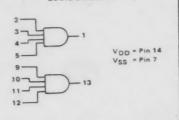
L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or efectric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < (Vin or Vout) < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).



Adv

QUAD

The MC146 and N-channel structure. The pation and/or be used in pation and waveforms.

- Quiescent
- Supply Vc
- Capable of Schottky ature Range
- Double D
- · Pin-for-Pi
- Can be U:

MAXIMUM RATIN

DC Supply Voltage Input Voltage, All In: DC Current Drain per Operating Temperatur

Storage Temperature

This device of static voltages taken to avoid this high imper Vout be constituted input either VSS or

CI

This is advance infor



2B 🗚

1

TARY MOSI

D" GATE

SUFFIX

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Package ckage Operating ture Range Operating ure Range

= Pin 14

protect pigh static ver, it is be taken ge higher this high eration it Vout be (Vin or

IC PACKAGE

MOTOROLA

МС14093В энтраля

Advance Information

QUAD 2-INPUT "NAND" SCHMITT TRIGGER

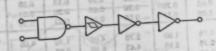
The MC14093B Schmitt trigger is constructed with MOS P-channel The MC140938 Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B 36

M RATINGS (Voltages referen

MAXIMUM RATINGS (Voltages referenced	Symbol	Value	Unit
Rating - 1 L0:	0,111	-0.5 to +18	Vdc
DC Supply Voltage	VDD	-0.5 to VDD + 0.5	Vdc
Input Voltage, All Inputs	Vin	10	mAdo
DC Current Drain per Pin	0 20.4	-55 to +125	°C
Tamperature Range - AL Device	E-1000 TT	-40 to +85	- 1
CL/CF Device	Tstg	-65 to +150	°C
Storage Temperature Range	- 11 1. 219	0.1	

EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



This device contains circuitry to protect the Inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} \leq (V_{in} or V_{out}) \leq V_{DD}. V_{out} be constrained to the range V_{SS} \leq (V_{in} or V_{out}) \leq V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

This is advance information and specifications are subject to change without notice.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" SCHMITT TRIGGER





I SUFFIX CERAMIC PACKAGE CASE 632

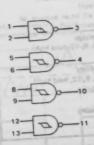
PSUFFIX PLASTIC PACKAGE CASE 646

ORDERING INFORMATION

Suffix Denotes MC14XXXB

L Ceramic Package P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

LOGIC DIAGRAM



VDD = Pin 14 Vss + Pin 7 net nigrata saleit



MC14528B

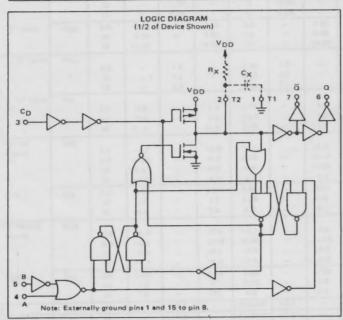
DUAL MONOSTABLE MULTIVIBRATOR

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X .

- Separate Reset Available
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- See MC14538B Data Sheet for Applications Requiring Precise Control of Output Pulse Width

MAXIMIM RATINGS (Voltages referenced to Voc.)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to VDD + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	оС
Storage Temperature Range	Tstg	-65 to +150	°C



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR



CERAMIC PACKAGE

PLASTIC PACKAGE

CASE 620

CASE 648

ORDERING INFORMATION

MC14XXXB Suffix Denotes L Ceramic Package
 P Plastic Package
 A Extended Operating Temperature Range Limited Operating Temperature Range

BLOCK DIAGRAM

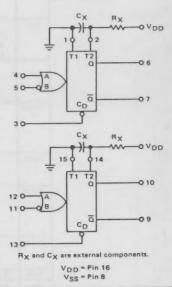


FIGURE 1 - OUTPUT SOURCE CURRENT TEST CIRCUIT

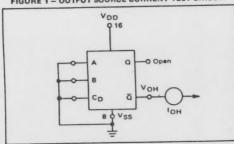


FIGURE 2 - OUTPUT SINK CURRENT TEST CIRCUIT

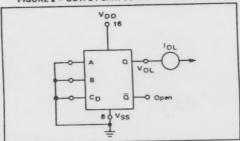


FIGURE 3 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

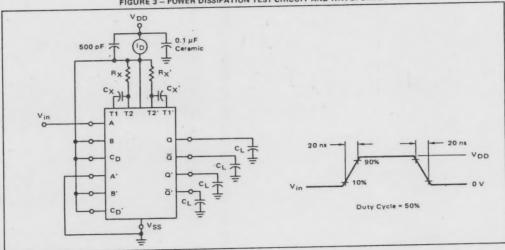


FIGURE 4 - AC TEST CIRCUIT

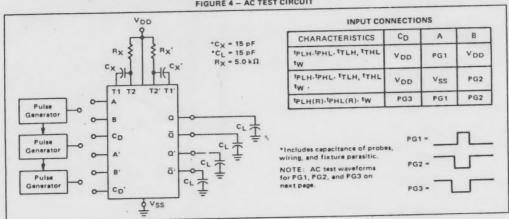
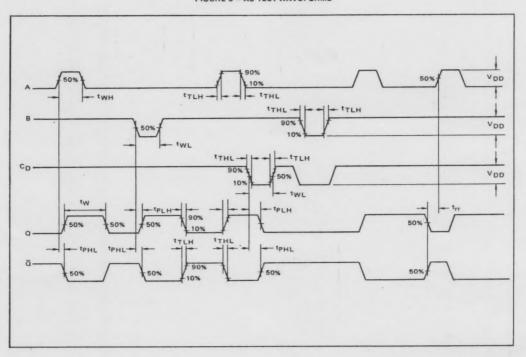
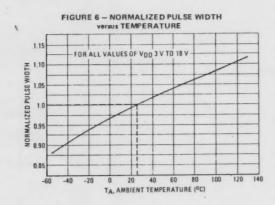
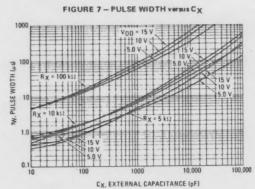


FIGURE 5 - AC TEST WAVEFORMS









DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, $C_{\boldsymbol{\chi}}$ and $R_{\boldsymbol{\chi}}$. Linear CMOS techniques allow more precise control of output pulse width.

- ±1.0% Typical Pulsewidth Variation from Part to Part
- ±0.5% Typical Pulsewidth Variation over Temperature Range
- New Formula: T = RC (T in seconds, R in ohms, C in farads)
- Pulse Width Range = 10 μs to ∞
- Symmetrical Output Sink and Source Capability
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- Quiescent Current (Standby) = 5.0 nA/package typical @ 5 Vdc
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive or Negative-Going Edge
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Tempera-
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- For Pulse Widths Less Than 10 μs the MC14528B is Recommended

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DĆ Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to VDD + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range – AL Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	Tstg	-65 to +150	oC.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

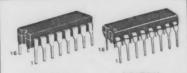
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

MC14538B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

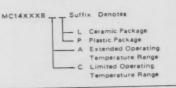
DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR



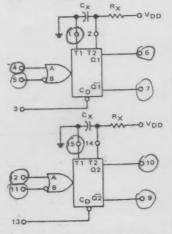
LSUFFIX CERAMIC PACKAGE CASE 620

PLASTIC PACKAGE CASE 648

ORDERING INFORMATION



BLOCK DIAGRAM



Rx and Cx are external components.

V_{DD} = Pin 16 V_{SS} = Pin 8, Pin 1, Pin 15

MC14538B

ELECTRICAL CHARA

Characteris

Output Voltage Vin = VDD or 0

Vin = 0 or VDD

Input Voltage

(V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (Vo = 13.5 or 1.5 Vdc

(Vo = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)

Output Drive Current (AL (VOH = 2.5 Vdc)

(VOH = 4.6 Vdc) (VOH = 9.5 Vdc)

(VOH = 13.5 Vdc)

(VOL = 0.4 Vdc) (VOL = 0.5 Vdc) (VOL = 1.5 Vdc)

Output Drive Current (CL

(VOH = 2.5 Vdc)

(VOH = 4.6 Vdc) (VOH = 9.5 Vdc) (VOH = 13.5 Vdc)

(VOL = 0.4 Vdc)

(VOL = 0.5 Vdc) (VOL = 1.5 Vdc)

Input Current, Pin 2 or 1 Input Current, Other Input Input Current, Other Inp Input Capacitance, Pin 2

Input Capacitance, Other (Vin = 0) Quiescent Current (AL D

(Per Package) Quiescent Current (CL/ (Per Package)

Quiescent Current, Activ (Q1 = Logic 1)

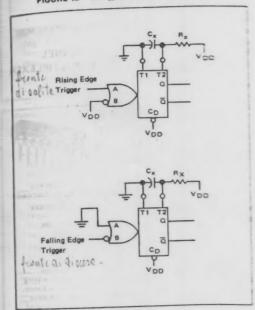
(Q2 = Logic 0) **Total Supply Current capacitance (CL) timing network IF

"Tlow = -55°C for AL L Thigh = +125°C for Al *Noise immunity specifi Noise Margin both "1"

**The formulas given ar

TYPICEL APPLICATIONS

FIGURE 12 — Retriggerable Monostables Circustry.



Rising Edge Trigger. Falling Edge Trigger

FIGURE 13 - Non-retriggerable Monostables Circuitry

om T = RxCa es the proper

not antifercaped

88235

this rate.

quation:

e of VDD to zero vota ustain damage. To avoid sistor, Rp, can be placed in 2 (or 14) of the derice from the capacitor to the

ection diode is equivalent

ected in series between a forward drop of 0.825 Ω . Int to 10 mA under con-

of pin 16 from VDD to

FIGURE 14 - Reduction of Power-Up Output Pulse Wighth

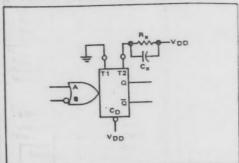


FIGURE 15 - Connection of Unused Sections